Diverse Instability Behaviors for N-Channel Low-Temperature Polycrystalline Silicon Thin Film Transistors
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Abstract
In this paper, the instability mechanisms and the diverse behaviors of n-channel LTPS TFTs under various bias stress conditions have been investigated. Statistically, it was found that TFTs present the highest standard deviation under $V_{gs} = 12.5 \, V$ and $V_{ds} = 20 \, V$. This was because the carriers gained energy to break only weak Si-Si bonds, reflecting the different effects of the various grains on the hot carrier effects. Discussion of the variations in different bias stress conditions is helpful in determining the lifetime prediction of the system-on-panel (SOP) design.

1. Introduction
Low-temperature poly-Si (LTPS) thin film transistors (TFTs) are widely used in addressing components in active matrix liquid crystal displays (AMLCDs) and system on glass (SOG) [1]. In the future, the application fields of LTPS TFTs will not be limited to displays but will be expanded to other electronic devices, such as LSIs, printers and sensors. In order to realize these new applications for TFTs, we have to enhance mobility, decrease the threshold voltage of TFTs, and the TFTs size. However, poly-Si TFT reliability improvements are critical for the insurance of the product lifetime. There are several kinds of degradation phenomena in poly-Si TFTs have already been reported.

Glass substrate is a poor thermal-conducting substrate and heat generated during the device operation is barely released. As a result, the device temperature can rise to a level that causes bonds to break. Such a phenomenon is called “self-heating” [2]-[5]. The degradation rate caused by self-heating depends on the operating power and the capability of heat dissipation of the device. In general, wide-channel TFTs or small-scale TFTs suffer from serious self-heating.

Hot carrier effects [6],[7] that originate from the high electric field near the drain junction have been widely investigated in LTPS TFTs. Conduction carriers can obtain energy from the high electric field and become “hot”. Thus, such high energy carriers can easily break the weak bonds existing in poly-Si, creating many defect states and oxide charges. Serious degradation can be generated in the hot carrier operation mode, and the degree of degradation depends on the strength of the electric field. Introducing electric-field-relief TFT structures, such as lightly doped drain (LDD), offset drain, and gate-drain overlapped LDD (GO-LDD), can reduce the hot carrier degradation.

However, the defects in the polysilicon films may leads to the deviation of the degrading speed. In this paper, the instability behaviors for LTPS TFTs are investigated statistically.

2. Device Fabrication and Experiment
The process flow of fabricating LTPS TFTs is described as follows. First, the buffer oxide and a-Si:H films were deposited on glass substrates, then XeCl excimer laser was used to crystallize the a-Si:H film, followed by poly-Si active area definition. Subsequently, a gate insulator was deposited. Next, the metal gate formation and source / drain doping were performed. A Lightly doped drain (LDD) structure was used on the devices. Dopant activation and hydrogenation were carried out after interlayer deposition. Finally, contact holes formation and metallization were performed to complete the fabrication work.

![Fig. 1. Schematic cross-section structure of the poly-Si TFT with lightly doped drain (LDD).](image)
The cross-section structure of the poly-Si TFT with LDD is illustrated in Fig. 1. We can observe the TFT is n-channel TFT.

In the experiment, we control different DC bias stress conditions were applied to the nominally identical LTPS TFTs with channel width and length \( W / L = 20\mu m / 6\mu m \) for the stress time up to 1000s. Many electric characteristics of the TFTs were measured before at the same condition.

3. Results and Discussion

Fig. 2. shows one example data of total measure data. It illustrates the sub-threshold characteristics of the n-channel TFTs with the application stress condition of \( V_{gs} = 15 \) V and \( V_{ds} = 20 \) V for different stress time.

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Fig. 3. shows the dependence of the mobility ratio \( \mu/\mu_0 \) on different stress times under the varying bias stress conditions. For the bias stress conditions, \( V_{ds} = 20 \) V was applied while the \( V_{gs} \) was varied from 10 V to 20 V for 1000s.

When the condition of \( V_{gs} = 10 \) V and \( V_{ds} = 20 \) V, the electric field near the drain side began to show the hot carrier effect. Due to the TFTs with LDD structure, the electric field was subsequently suppressed and thus the degradation was not severe. When the condition of \( V_{gs} = 15 \) V and \( V_{ds} = 20 \) V, the lateral electric field became maximum [8],[9]. The hot carrier stress was the most severe, therefore, the degradation was the worst. Since the lateral electric field was small when the condition of \( V_{gs} = V_{ds} = 20 \) V, the degradation was negligible due to the insignificant amount of hot carriers.

Furthermore, the diversity of devices under the same bias stress condition can also be observed in Fig. 3. Two conditions with the same \( V_{ds} = 20 \) V of \( V_{gs} = 12.5 \) V and \( V_{gs} = 17.5 \) V were chosen as the bias stress conditions for further discussion.

As can be seen in Fig. 5., when the condition of \( V_{gs} = 17.5 \) V, due to the high current effect, self-heating effect became observable and the degradation was severe. Furthermore, Fig. 4. and Fig. 5. also show that variations in different devices were pronounced under these two bias stress conditions with \( V_{ds} = 20 \) V of \( V_{gs} = 12.5 \) V and \( V_{gs} = 17.5 \) V. This phenomenon will be explained and discussed later.
Fig. 6. presents the standard deviations among different devices under these bias stress conditions. When the condition of $V_{gs} = 10$ V, the standard deviation is small. This is due to the small electric field near the drain side region that creates much fewer hot carriers compared to the case for other bias stress conditions. Since the degradation is not severe, this explains why the variation is small.

When the condition of $V_{gs} = 12.5$ V, the standard deviation is the largest under the different stress times. This is because the weak Si-Si bonds in the grains and dangling bonds at the grain boundaries. Furthermore, the hydrogenation process also creates a large amount of weak Si-H bonds in poly-Si film. These weak bonds can easily be broken under the device operation.

Some circumstances were the carrier just get the energy which only can break the weak Si-H bonds and some circumstances were the carrier get the energy which can not break the weak Si-H bonds. As a result, when the condition of $V_{gs} = 12.5$ V, the standard deviation is the largest.

Fig. 7. shows different TFTs with various amount of grain boundaries existing in the channel. This will result in the variation of the device characteristics [9],[10]. Therefore, the degradation behaviors of TFTs are very different. When the condition of $V_{gs}$ was increased to 15 V, these hot carriers near the drain side obtained enough energy to break not only weak Si-Si and Si-H bonds but nearly all of the Si-Si and Si-H bonds at grain boundaries.

Hence, the variation under this condition of $V_{gs} = 15$ V was less than the condition of $V_{gs} = 12.5$ V. As the stress time was increased, most bonds at grain boundaries were broken so that the standard deviation decreased.

When the condition of $V_{gs} = 17.5$ V, the standard deviation decreased and then increased. This phenomenon may be due to the fact that holes inject into the buffer oxide, causing the short-channel effect [11],[12]. As the stress times increase, the mobility ratio $\mu/\mu_0$ is increased. It is
because when the stress time increase the TFTs devices were similar under the circumstance of “anneal”.

When the condition of $V_{gs} = 20$ V, the standard deviation was the smallest because the electric field in the channel under this condition was weak and the degradation was not severe.

4. Conclusions
The reliability and variation of n-channel LTPS TFTs under various bias stress conditions have been investigated in this paper. Such effects can be ascribed to the variations of the Si-Si dangling bonds under the medium hot carrier conditions due to the different grain structures. The discussion of variations in different bias stress conditions is inevitable for SOG applications.

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